

REMARKS

The Office Action dated March 26, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-12, 14-23, 25-35, 37-38, and 40-42 are pending in the present application. Claims 1, 14-16, 20, 25-27, 31, 35, 37, and 40-41 are independent claims. Claims 1-12, 14, 20-23, 25, 31-34, 37-38, and 41-42 having been allowed, claims 15-19, 26-30, 35, and 40 are respectfully submitted for consideration.

As a preliminary matter, Applicants thank the Examiner for explaining to Applicants' undersigned representative via telephone that page 3 of the outstanding Office Action contains a typographical error and that claim 40, not claim 39, is rejected. Applicants also thank the Examiner for clarifying that claim 41 is allowed.

Rejection of Claims 15, 26, and 40 Under 35 U.S.C. § 103(a):

Claims 15, 26, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,157,643 to Ma (Ma '643). Although it is acknowledged in the Office Action that Ma '643 fails to disclose a predetermined number of stack link interfaces that are configured to be one less than a predetermined number of switch building blocks, it is alleged in the Office Action that such a configuration is obvious as a matter of design choice. Also, although it is acknowledged in the Office Action that Ma '643 fails to disclose storing a packet in a memory in accordance with a predetermined algorithm, it is alleged in the Office Action that Ma '643 discloses using

buffers to receive packets. It is further alleged in the Office Action that, since such a buffer is used for temporary storage, it would have been obvious to one skilled in the art that an algorithm must be used to control the storage of packets in the buffers. This rejection is respectfully traversed.

Claim 15 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch buildings blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. Also, the predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 16 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. Also, the at least one data port interface includes at least one first data

port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 40 recites a method of handling packets in a network switch. The method includes the steps of receiving a packet in a clustered network switch, determining a destination address of the packet from a lookup operation in a common table, and forwarding the packet to the destination address determined from the lookup operation. The receiving step further includes the steps of receiving a packet on at least one of a data port interface and a stack link interface and storing the packet in a memory in accordance with a predetermined algorithm.

As discussed in the present specification, an advantage of the claimed invention is that it provides numerous options for combinations of port speeds and logical port connectivities. It is respectfully submitted that the referenced cited in the Office Action, whether viewed individually or in combination, fail to disclose or suggest the elements of any of the presently pending claims. Therefore, it is respectfully further submitted that the references cited in the Office Action fail to provide at least the advantages discussed above.

Ma '643 discloses "a switching fabric for a packet-switched communications network" (lines 1-2 of the Abstract thereof). In Figure 2 thereof, Ma '643 also discloses a "structure of a three-stage Clos network having both the first and third stage comprised of k switch elements" (column 5, lines 45-47). Ma '643 further discloses that "the number

of alternative paths between switch input i and output j is equal to the number of internal stage switch elements” (column 6, lines 16-18).

However, Ma ‘643 fails to disclose or suggest at least “a predetermined number of stack link interfaces . . . [that] is configured to be one less than the predetermined number of switch building blocks,” as recited in claims 15 and 26 of the present application. Ma ‘643 also fails to disclose or suggest at least “determining a destination address of the packet from a lookup operation in a common table,” as recited in claim 40 of the present application.

In the Office Action, it is alleged that the configuration of the “predetermined number of stack link interfaces” recited in claims 15 and 26 is obvious as a matter of design choice. However, Applicants respectfully submit that a *prima facie* case of obviousness has not been properly established in the Office Action.

As set forth in MPEP § 2143, “[t]o establish a *prima facie* case of obviousness. . . there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference.” In the present instance, Applicants respectfully submit that one of skill in the art, upon reading Ma ‘643, would understand that the switching fabric disclosed therein need not include the configuration of stack link interfaces recited in claims 15 and 26 of the present application to operate in the communications network disclosed in Ma ‘644. Further, Applicants submit that one of skill in the art would understand that including the configuration recited in claims 15 and 16 would add additional costs and complexity to

the switching fabric disclosed in Ma '643. Therefore, Applicants point out that one of skill in the art would not be motivated to modify Ma '643 as suggested in the Office Action.

With respect to claim 40, it is alleged in the Office Action that the step of "determining a destination address of the packet from a lookup operation in a common table," recited therein is necessarily present in Ma '643 because, to switch, one needs to know to which output to direct the packet. Applicants respectfully disagree.

Applicants point out that, according to the related art, in order to switch, information concerning to which output to direct a packet need not involve the use of the "common table" recited in claim 40 of the present application. For example, a plurality of tables could be used to perform a lookup operation. Therefore, Applicants further point out that at least the "determining" step recited in claim 40 is neither disclosed nor suggested by Ma '643.

At least in view of the above, Applicants respectfully submit that Ma '643 fails to disclose or suggest the subject matter recited in claims 15, 26, and 40 of the present application. Therefore, Applicants further submit that claims 15, 26, and 40 are patentable over Ma '643 and respectfully request reconsideration and withdrawal of the rejection of claims 15, 26, and 40 under 35 U.S.C. § 103(a) as being unpatentable over Ma '643.

Rejection of Claims 16-18 and 27-29 Under 35 U.S.C. § 103(a):

Claims 16-18 and 27-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma '643 in view of U.S. Patent No. 6,226,292 B1 to DiPlacido (DiPlacido '292). It is acknowledged in the Office Action that Ma '643 fails to disclose first and second ports supporting a plurality of first and second data ports transmitting/receiving data at first and second rates. However, it is alleged in the Office Action that DiPlacido '292 discloses fast Ethernet and gigabit inputs that represent different rates. It is also alleged in the Office Action that Ma '643 and the DiPlacido '292 may be combined to yield the present claimed invention. This rejection is respectfully traversed.

Claim 16, upon which claim 17-18 depend, recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data and a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. The at least one data port interface also includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 27, upon which claims 28-29 depend, recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. Each of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data and a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. The at least one data port interface also includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data interface supporting at least one second data port transmitting and receiving data at a second rate.

As discussed previously, among the advantages of the claimed invention are that numerous options for combinations of port speeds and logical port connectivities are available.

Ma '643 discloses a switching fabric wherein "each routing network element routes the data packets according to preset, fixed rules" and "within a given time slot" (line 16-18 and 21-22 of the Abstract). However, Ma '643 fails to disclose or suggest at least the "at least one data port interface...[which] further comprises...at least one first data port interface...receiving data at a first data rate; and at least one second data port interface...receiving data at a second rate," as recited in claims 16 and 27 of the present application.

DiPlacido '292 discloses, in the title thereof, "frame replication in a network switch for multi-port frame forwarding". DiPlacido '292, in Figure 1 thereof, also discloses "Gigabit Ethernet links" and "fast Ethernet links". However, Applicants respectfully submit that DiPlacido '292 is not properly combinable with Ma '643.

As mentioned above, Ma '643 discloses a switching fabric that makes use of time slots to route data packets therethrough. However, Ma '643 fails to disclose or suggest that these time slots may be varied in length. Therefore, Applicants respectfully submit that the switching fabric disclosed in Ma '643 would be incapable of supporting more than a single data rate.

More specifically, since the time slots disclosed in Ma '643 and used to operate the switching fabric disclosed therein are of a given length, multiple data rates would fill different time slots with different amounts of data. Since the switching fabric disclosed in Ma '643 is neither disclosed nor suggested as being able to accommodate time slots with different amounts of data, Applicants respectfully submit that modifying Ma '643 to include the fast Ethernet and Gigabit Ethernet links disclosed in DiPlacido '292 would render the switching fabric disclosed in Ma '643, at best, unsatisfactory for its intended purpose and, at worst, completely inoperable. Therefore, since such a modification is prohibited under MPEP § 2143.01, Applicants respectfully submit that there is no suggestion or motivation to include the subject matter recited in DiPlacido '292 in Ma '643.

At least in view of the above, Applicants respectfully submit that Ma '643 and DiPlacido '292 may not properly be combined. Therefore, Applicants further submit that claims 16-18 and 27-29 are patentable over Ma '643 and DiPlacido '292 and respectfully request reconsideration and withdrawal of the rejection of claims 16-19 and 27-29 under 35 U.S.C. § 103(a) over Ma '643 in view of DiPlacido '292.

Rejection of Claim 35 Under 35 U.S.C. § 103(a):

Claim 35 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma '635 in view of U.S. Patent No. 6,195,334 B1 to Kadambi et al. (Kadambi '334). In the Office Action, it has been acknowledged that Ma '643 fails to disclose a physical layer transceiver in connection with at least one of a plurality of data ports. However, in the Office Action, it is alleged that Kadambi '334 discloses a network switch including a physical layer transceiver and that it would have been obvious to one of ordinary skill in the art to combine Kadambi '334 with Ma '643 to yield the present claimed invention. This rejection is respectfully traversed.

Claim 35 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. Each of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data and a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number

of building blocks. The scalable network switch also includes a physical layer transceiver in connection with at least one of the plurality of data ports.

As discussed above, the claimed invention has as an advantage thereof that numerous options for combinations of port speeds and logical port connectivities are available.

Ma '643 discloses that it "concerns a switching fabric employed in such a communications network, especially, an ATM network" (column 1, lines 10-12). Ma '643 also discloses that in "an ATM network, the problems of conventional packet-switched networks...are overcome by transmitting short packets of a constant length" (column 1, lines 53-55). In direct contrast, Applicants point out that Kadambi '334 discloses "controlling internal data transfers in a network switch for a half-duplex Ethernet...packet switched network (column 1, lines 9-11). Kadambi '334 also discloses "filtering collision fragments and runt packets" (column 2, line 6).

Applicants respectfully submit that the switching fabric disclosed in Ma '643 is designed specifically to utilize the advantages that constant length packets provide. Applicants also respectfully submit that Kadambi '334 is specifically designed to accommodate the use of packets that are not of a constant length. Therefore, Applicants further submit that the suggestion or motivation to combine Ma '643 and Kadambi '334 necessary to establish a *prima facie* case of obviousness, as discussed in MPEP § 2143, is not present in this instance. At least in view of the above, Applicants respectfully submit that the combination of Ma '643 and Kadambi '334 is improper and

that a *prima facie* case of obviousness has not been properly established against claim 35 of the present application.

At least for the above reasons, Applicants respectfully submit that claim 35 is patentable over Ma '643 and Kadambi '334, taken either individually or in combination. Therefore, reconsideration and withdrawal of the rejection of claim 35 under 35 U.S.C. § 103(a) over Ma '643 in view of Kadambi '334 is respectfully requested.

Allowable Subject Matter:


Applicants thank the Examiner for acknowledging that claims 1-12, 14, 20-23, 25, 31-34, 37-38, and 41-42 are allowed. Applicants also thank the Examiner for acknowledging that claims 19 and 30 contain allowable subject matter.

Applicants respectfully submit that all of the issues raised in the Office Action have been addressed and that all of the rejections included in the Office Action have been overcome. Therefore, Applicants respectfully further submit that all of claims 1-12, 14-23, 25-35, 37-38, and 40-42 of the present application contain allowable subject matter. Thus, it is respectfully requested that all claims pending in the present application be allowed, and that this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,


Hermes M. Soyez, Ph.D.
Registration No. 45,852

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

HMS:mm